In the Claims:

Please amend Claims 3, 6, 9-10, 13, 17-20, 23-24 as follows:

Claim 1-2 (Previously cancelled).

Claim 3. (Currently Amended) A computer system comprising:

a host processor;

a peripheral device configured to transfer data from a network to the host processor over an attachment bus inside the computer system using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is configured to receive data during time cycles ~~periods~~ of predetermined length; where the control circuit is configured to place at least a minimum amount of data from the first queue onto the bus during each time cycle ~~period~~; where the control circuit is configured to place data from the second queue onto the bus only when the bus is otherwise unoccupied by first class data.

Claim 4. (Previously Amended) The system of claim 3, where the peripheral device includes a network interface component connected to receive the data from a computer network.

Claim 5. (Previously Amended) The system of claim 3, wherein the data includes packetized voice data.

Claim 6. (Currently Amended) A computer system comprising:

a host processor;

a peripheral device configured to transfer data to the host processor over an attachment bus inside the computer system using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is a Universal Serial Bus (USB), and the first type of transfer associated with the first class of data ~~peripheral device~~ is ~~configured to transfer data over the bus using~~ an isochronous transfer, and the second type

of transfer associated with the second class of data is a ~~and~~ bulk transfer~~transfers~~.

Claim 7. (Previously Amended) The system of claim 3, where the peripheral device is configured to deliver the data in packets of predetermined length.

Claim 8. (Previously Amended) The system of claim 7, where the classifying circuit is configured to place each of the packets into one of the queues.

Claim 9. (Currently Amended) A computer system comprising:

a host processor;

a peripheral device configured to transfer data from a network to the host processor over an attachment bus inside the computer system using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is configured to receive data during time cycles of predetermined length;~~The system of Claim 7,~~ where a portion of each packet indicates a virtual channel

associated with the packet, and where the classifying circuit includes a storage device that stores information indicating each of the virtual channels that is associated with at least one of the classes.

Claim 10. (Currently Amended) The system of claim 9, where the classifying circuit includes a selection element configured to (a) compare, for each packet, the information in the storage device to the data in the portion of the packet that indicates a virtual ~~the~~ channel and ~~configured to~~ (b) select a corresponding one of the queues to receive the packet.

Claim 11-12 (Previously cancelled).

Claim 13. (Currently Amended) A method comprising:

transferring data from a network to a host processor over an attachment bus inside the computer system using at least first and second types of data transfers and, in transferring the data:

separating the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer; ~~and~~

placing data of the first class onto the bus at a higher priority than data of the second class is placed onto the bus;[.]

placing data on the bus during time cycles ~~periods~~ of predetermined length, where placing data of the first class on the bus includes placing at least a minimum amount of data of the first class onto the bus during each time cycle ~~period~~; and

placing data of the second class onto the bus only when the bus is otherwise unoccupied by first class data.

Claim 14. (Previously Amended) The method of claim 13, further comprising receiving the data from a computer network.

Claim 15. (Previously Amended) The method of claim 13, where receiving the data includes receiving packetized voice data.

Claim 16. (Previously Amended) The method of claim 13, where transferring data includes delivering the data in packets of predetermined length.

Claim 17. (Currently Amended) The method of claim 16~~11~~, where separating the data includes placing each of the packets into one of a plurality of~~the~~ queues.

Claim 18. (Currently Amended) A method comprising:

transferring data from a network to a host processor over an attachment bus inside the computer system using at least first and second types of data transfers and, in transferring the data:

separating the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

placing data of the first class onto the bus at a higher priority than data of the second class is placed onto the bus;

placing data on the bus during time cycles of predetermined length; and

~~The method of claim 11, further comprising~~ storing information indicating each virtual channel that is associated with at least one of the classes.

Claim 19. (Currently Amended) The method of claim 18, further comprising:

comparing, for each packet, the stored information to a portion of the data in the packet that indicates the virtual channel associated with the packet; and

placing the packet into a corresponding one of the queues.

Claim 20. (Currently amended) The system of claim 9, where the classifying circuit comprises a buffer adapted to buffer a received packet, a shift register adapted to store a portion of the received packet, and the storage device is a content addressable memory (CAM) device adapted to store information indicating each of the virtual channels that is associated with at least one of the classes.

Claim 21. (Previously added) The system of claim 3, wherein the bus is a Peripheral Component Interface (PCI) bus.

Claim 22. (Previously added) The system of claim 3, wherein the bus uses an Asynchronous Transfer Mode (ATM).

Claim 23. (Currently amended) A peripheral device coupled between a host device and a network, the peripheral device operable to transfer data packets from the network to the

host processor over a bus inside the computer system, the peripheral device comprising:

a classifying circuit operable to identify a priority level of each data packet from the network;

a first queue operable to store data packets with a first priority level from the classifying circuit;

a second queue operable to store data packets with a second priority level from the classifying circuit; and

a control circuit coupled to first and second queues, the control circuit being operable to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is configured to receive data during time cycles ~~periods~~ of predetermined length; the control circuit being configured to place at least a minimum amount of data from the first queue onto the bus during each time cycle ~~period~~; the control circuit being configured to place data from the second queue onto the bus only when the bus is otherwise unoccupied by first class data.

Claim 24. (Currently amended) A peripheral device coupled between a host device and a network, the peripheral device operable to transfer data packets from the network to the host processor over a bus, the peripheral device comprising:

a classifying circuit operable to identify a priority level of each data packet from the network;

a first queue operable to store data packets with a first priority level from the classifying circuit;

a second queue operable to store data packets with a second priority level from the classifying circuit; and

a control circuit coupled to the first and second queues, the control circuit being operable to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is a Universal Serial Bus (USB), and the first type of transfer associated with the first class ~~peripheral device~~ is ~~configured to transfer data over the bus using~~ an isochronous transfer, and the second type of transfer associated with the second class is a ~~and~~ bulk transfer ~~transfers~~.